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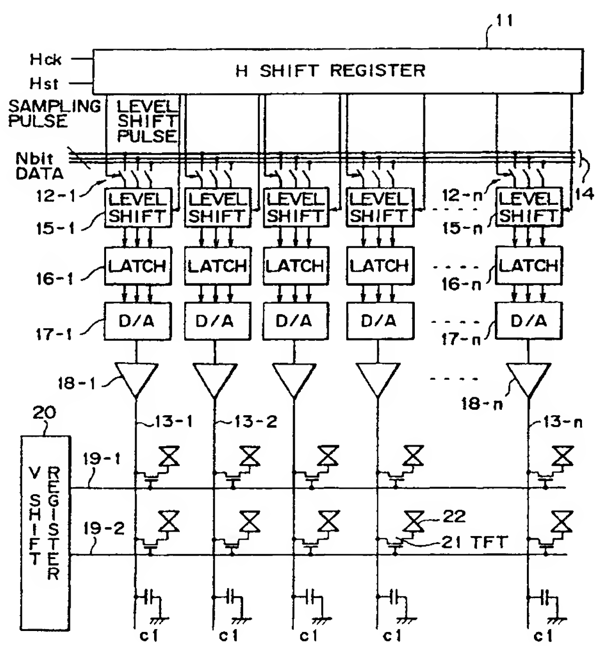
(54) **Data driver for an active liquid crystal display device**

(57) In an active matrix type LCD having a driving circuit unit which is capable of accepting digital signals having a signal level lower than the power source voltage of a horizontal driving circuit system combined with pixel unit, level shift circuits (15-1 to 15-n) for converting the level of sampled digital signals having a small amplitude to digital signals having a voltage of 0 to the power source voltage Vd are provided between sampling switches (12-1 to 12-n) and latch circuits (16-1 to 16-n). The structure is thus capable of accepting from the outside digital signals having a small signal amplitude and can be applied to a medium to large sized LCD.

F I G. 1



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Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] This invention relates to a liquid crystal display (LCD) device, and more particularly relates to an active matrix type liquid crystal display device having a combination of a driving circuit unit and a pixel unit which is capable of accepting a digital signal having a signal level lower than a power source voltage level of a horizontal driving circuit system.

Description of Related Art

[0002] Recently, the trend that LCD monitors separated from notebook type personal computers (referred to as personal computer hereinafter) are used as desktop type monitors has become accentuated in response to the development of thin LCD monitors of reduced power consumption. The internal circuit of a personal computer is structured so that digital signals are processed. On the other hand, a CRT monitor is driven by analog signals, and therefore the input output I/F (interface) is an analog I/F. However, because a LCD itself of a-Si uses mainly a source driver IÇ of a digital I/F, A/D conversion should be performed again somewhere. Such conversion is very inefficient for the whole system.

[0003] In such background, as for the state of the art of the driving circuit combined type LCD, merely a sampling system of an analog video signal as shown in FIG. 5 has been developed. A circuit having a digital I/F has not been realised. Herein, the system in accordance with the conventional example shown in FIG. 5 is described. Between a signal line 101 for transmission of an analog video signal and column lines 102-1 and 102-n, n transfer gates 103-1 to 103-n are connected.

[0004] These transfer gates 103-a to 103-n are turned on (i.e. become conductive) at the rising edge of sampling pulses Ø1, Ø2, ..., Øn supplied successively from the H shift register 104 to sample an analog video signal, which is supplied successively to column lines 102-1 to 102-n. On the other hand, m row lines 105-1 to 105-m are driven successively by the V shift register 106.

[0005] On respective intersection points of n column lines 102-1 to 102-n and m row lines 105-1 to 105-m, a thin film transistor (TFT) is provided. A source electrode of the thin film transistor 107 is connected to a column line 102-1 to 102-n, a gate electrode is connected to a row line 105-1 to 105-n respectively. A drain electrode of the thin film transistor 107 is connected to the transparent pixel electrode of pixels 108 respectively arranged two dimensionally in the form of a matrix.

[0006] The system in accordance with the conventional example having the structure described herein above is advantageous for a small sized LCD of, for example, the view finder of a video camera or the light bulb of a projector in that a full colour (full analog) display is realised with a relatively simple structure. However, application to a large sized or medium sized LCD results in a significant disadvantage.

(1) Use of a large sized LCD panel inevitably leads to use of large capacity video line and source line (column line), and a large power is consumed when signals are charged/discharged rapidly. Further, an analog buffer for driving such load results in very large EMI (Electromagnetic Interference) source, and set design is difficult.

(2) It is considered in order to cope with the problem (1) that an analog signal is divided into a multiplicity of divided signals and divided analog signals are supplied. However it is very difficult to eliminate the dispersion between channels of a multiplicity of divided analog signals. Further, the system will be a very complex and large system.

(3) Point-successive sampling timing and phase control of video signals are very difficult and the image quality inevitably becomes poor due to ghost.

[0007] For the reason described herein above, a large sized driving circuit combined LCD has not been realised up to today. In the field of a-Si (amorphous silicon) LCD, heretofore a method in which a silicone LSI is mounted near a panel using mounting method of TAB (Tape Automated Bonding) and a signal is supplied is employed. However, cost of silicon LSI and mounting cost of a silicon LSI results directly in an increased panel cost.

SUMMARY OF THE INVENTION

[0008] The present invention is accomplished in view of overcoming such problem. It is the object of the present invention to provide a driving circuit combined type liquid crystal display device which is capable of simplifying the interface with a personal computer and accepting digital input.

[0009] The liquid crystal display device according to the invention is a liquid crystal display device having a combination of a driving circuit unit and pixel unit which is capable of accepting a digital signal input having a signal level lower than a power source voltage level of a horizontal driving circuit system, comprising a pulse generation means for generating a sampling pulse which samples in time series an input digital signal correspondingly to a pixel, a sampling means for sampling the input digital signal in response to the sampling pulse, a level conversion means for converting a digital signal sampled by the sampling means to a signal having a signal level sufficient for subsequent processing, and a D/A conversion means for generating an analog signal based on a digital signal which was level converted by the level conversion means.

[0010] In the above-mentioned liquid crystal display

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element, the driving circuit unit includes a system for sampling digital signals, a system for converting the level of sampled digital signals, and a system for converting digital signals to analog signals and the pixel unit are formed combinedly. The level of input digital signals with a small amplitude is converted to the power source voltage level of the horizontal driving circuit, and the liquid display element is thereby rendered capable of accepting from the outside digital signals having a small amplitude.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] FIG. 1 is a schematic structural diagram for illustrating one embodiment of the present invention.

[0012] FIG. 2 is a circuit diagram for illustrating one example of a detailed circuit structure of a level shift circuit and a latch circuit.

[0013] FIG. 3 is a timing waveform diagram for describing the operation of the circuit shown in FIG. 2.

[0014] FIG. 4 is a circuit diagram for illustrating a modified example of a level shift circuit and a latch circuit.

[0015] FIG. 5 is a schematic structural diagram for illustrating a conventional example.

[0016] FIG. 6 is a timing waveform diagram in accordance with the conventional example.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0017] Embodiments of the present invention will be described in detail hereinafter with reference to the drawings. FIG. 1 is a schematic structural diagram for illustrating one embodiment of the present invention. An active matrix type LCD in accordance with the present invention has a structure in which a pixel unit and a driving circuit unit for receiving a digital signal having a signal level lower than that of a power source voltage (Vd) of the horizontal driving circuit system are formed combinedly on a glass substrate. A digital signal to be supplied is a N bit digital data (for colour display, the number of total data lines is R, G, B × number of parallel processing)

[0018] In FIG. I, a shift register 11 which functions as a horizontal scanning circuit generates a sampling pulse for sampling an input digital data in time series correspondingly to a pixel based on a horizontal start pulse Hst and horizontal clock pulse Hck, and generates a level shift pulse as described hereinafter. A group of sampling switches 12-1 to 12-n is provided correspondingly to n column lines 13-1 to 13-n, and samples a digital data on a data bus line 14 in response to the sampling pulse supplied successively from the H shift register 11.

[0019] Digital data sampled successively by the group of sampling switches 12-1 to 12-n is supplied to level shift circuits 15-1 to 15-n which function as the level conversion means. The level shift circuits 15-1 to 15-n shift the signal level of respective sampling data to a power source voltage (Vd) level of a horizontal driving circuit system based on a level shift pulse given by the H shift register 11. Respective sampling data shifted by level shift circuits 15-1 to 15-n are held during one horizontal time period by latch circuits 16-1 to 16-n.

[0020] Respective latch data of latch circuits 16-1 to 16-n are converted to analog signals by D/A converters 17-1 to 17-n, and supplied to output buffers 18-1 to 18-n. Output buffers 18-1 to 18-n drive column lines 13-1 to 13-n based on analog signals given by D/A converters 17-1 to 17-n. On the other hand, m row lines 19-1 to 19-m are vertically scanned successively by a V shift register 20 which functions as a vertical scanning circuit and driver.

[0021] Respective intersection points of n column lines 13-1 to 13-n and m row lines 19-1 to 19-m have a thin film transistor (TFT) 21. The source electrode of a thin film transistor is connected to a column line 13-1 to 13-n and the gate electrode is connected to a row line 19-1 to 19-m respectively. The drain electrode of the thin film transistor 21 is connected to a transparent pixel electrode of liquid crystals (pixel) 22 which are arranged two dimensionally in the form of a matrix.

[0022] The above-mentioned driving circuit system comprising the H shift register 11, the group of switches 12-1 to 12-n, level shift circuits 15-1 to 15-n, latch circuits 16-1 to 16-n, D/A converters 17-1 to 17-n, output buffers 18-1 to 18-n, and the V shift register 20 is formed on a polysilicone or crystal silicone transparent substrate or silicone substrate.

[0023] FIG. 2 is a circuit diagram for illustrating one example of detailed circuit structure of a level shift circuit and latch circuit. In this drawing, one end of a switch 32 is connected to a digital data line 31 and the one ends of a switch 33 and capacitor 34 are connected respectively to the other end of the switch 32. The other end of the switch 33 is connected to a reference voltage line 35. A reference voltage Vref of the reference voltage line 35 is set to a voltage around (VH-VL)/2 wherein VH and VL stand for "H" level and "L" level of a digital data.

[0024] An input terminal of an inverter 36 and each one end of switches 37 and 38 are connected to the other end of the capacitor 34. The other end of the switch 37 and the input terminal of an inverter 39 are connected to the inverter 36. The other end of the switch 38 is connected to the output terminal of the inverter 39. In other words, the switch 37 is connected to the inverter 36 in parallel, and the switch 38 is connected in parallel to inverters 36 and 39 which are two step cascade connected.

[0025] In the above-mentioned circuit structure, respective shift circuits 15-1 to 15-n comprise the switch 33, capacitor 34, inverter 36, and switch 37, and respective latch circuit 16-1 to 16-n comprise the two step cascade connected inverters 36 and 39, and switch 38. The switch 32, switches 33 and 37, and switch 38 are on-off controlled in response to the sampling pulse, equalising pulse, and latch pulse respectively.

[0026] The sampling pulse and equalising pulse are equivalent to the sampling pulse and level shift pulse generated by the H shift register 11. The latch pulse is generated by the H shift register 11. As described herein above, the H shift register 11 for generating the horizontal scanning sampling pulse is served commonly as the pulse generation circuit for generating various pulses such as the level shift pulse and latch pulse, thereby the circuit structure of a whole system is simplified advantageously in comparison with use of exclusively separate pulse generation circuits.

[0027] Next, circuit operation of the level shift circuit and latch circuit having the structure described herein above is described with reference to timing wave form diagrams shown in FIG. 3.

[0028] First, in a data period immediately antecedent to a data period ("H" level period of sampling pulse) in which sampling is actually performed, an equalising pulse is changed to "H" level to turn on the switch 33. The capacitor 34 is thereby charged with the reference voltage Vref. The reference voltage Vref is served as a reference voltage for determining the level of digital data to be supplied next. Then, the switch 37 is turned on simultaneously to connect input/output terminals of the front end inverter 36, and the operation point is set to a value around intermediate voltage.

[0029] The equalising pulse is changed to "L" level, then the sampling pulse is changed to "H" level, the switch 32 is turned on, the digital data is thereby sampled. Then, whether the level of the supplied digital data is higher or lower than the reference voltage Vref is determined. If the digital data is higher, then the output level of the inverter 36 is changed to 0 V. On the other hand, if the digital data is lower, then the output level of the inverter 36 is changed to the power voltage Vd (for example 12 V) of the horizontal driving circuit system.

[0030] Then, the sampling pulse is changed to "L" level, the latch pulse is changed to "H" level. Hence, the switch 38 is turned on, and the front end inverter 36 and rear end inverter 39 are loop connected through the switch 38 to structure a latch circuit. As a result, the sampled digital data is held for one horizontal period as the output level of the inverter 39 in the condition that the level of the sampled digital data is shifted to the power source voltage Vd.

[0031] As described herein above, by providing level shift circuits 15-1 to 15-n between sampling switches 12-1 to 12-n and latch circuits 16-1 to 16-n, the sampled digital signal having a small amplitude (VH - VL) is amplified rapidly to a digital signal of 0 V to the power source voltage Vd (for example 12 V) namely a digital signal having a signal level required to process in latch circuits 16-1 to 16-n and subsequent circuits.

[0032] It is possible thereby to supply a digital signal having a small amplitude from the outside. By rendering the circuit structure acceptable to digital input, the interface to a personal computer is simplified. A level shift circuit and latch circuit having a circuit structure as shown in FIG. 4 may be used. In detail, in this modified example, an inverter 39 and switch 40 are connected in parallel. A circuit structure in which the switch 40 is on-off controlled in response to an equalising pulse together with a switch 37 is realised, and this circuit structure functions like the above-mentioned circuit structure.

[0033] In the above-mentioned embodiment, the case of a circuit structure in which the level shift circuits 15-1 to 15-n for shifting the level of the sampled digital signal to 0 V to the power source voltage Vd as a level conversion means are used is described. However alternatively, the level conversion means is by no means limited to this case, and other structures may be used as long as the structure performs level conversion or amplification of the sampled digital signal to a signal having a signal level sufficient for processing in latch circuits 16-1 to 16-n and subsequent circuits.

[0034] According to the present invention as described hereinbefore, by providing a means for converting the level of a sampled digital signal to a signal having a signal level sufficient for subsequent processing in a driving circuit unit and by forming the driving circuit unit and pixel unit combinedly, the combined system is rendered capable of accepting a digital signal input having a small signal amplitude from the outside, and thus the interface with a personal computer is simplified. Further, because a process for mounting a dedicated IC such as TAB used conventionally is unnecessary, the cost is reduced and the number of connection terminals is significantly reduced, and the reliability of mounting is greatly improved.

Claims

1. A liquid crystal display device having a combination of a driving circuit unit and a pixel unit which is capable of accepting a digital signal input having a signal level lower than a power source voltage level of a horizontal driving circuit system, comprising:

   pulse generation means (11) for generating a sampling pulse which samples in time series an input digital signal correspondingly to a pixel;
   sampling means (12-1 to 12-n) for sampling said input digital signal in response to said sampling pulse;
   level conversion means (15-1 to 15-n) for converting a digital signal sampled by said sampling means (12-1 to 12-n) to a signal having a signal level sufficient for subsequent processing; and
   D/A conversion means (17-1 to 17-n) for generating an analog signal based on a digital signal which was level converted by said level conversion means (15-1 to 15-n).

2. A liquid crystal display device according to claim 1,

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further comprising:

latch means (16-1 to 16-n) for holding a digital signal converted by said level conversion means (15-1 to 15-n).

3. The liquid crystal display device as claimed in claim 2, wherein said latch means (16-1 to 16-n) holds a digital signal during one horizontal period.

4. The liquid crystal display device as claimed in claim 2 or claim 3, wherein said level conversion means (15-1 to 15-n) and said latch means (16-1 to 16-n) comprise a first switch (32) the one end of which is connected to a digital data line (31), a second switch (33) the one end of which is connected to the other end of said first switch (32) and the other end of which is connected to a reference voltage (35), a capacitor (34) the one end of which is connected to the connection middle point of said first switch (32) and said second switch (33), a first inverter (36) connected to the other end of said capacitor (34), a third switch (37) provided between input and output of said first inverter (36) and controlled by a level shift pulse, a second inverter (39) connected to the output of said first inverter (36), and a fourth switch (38) connected in parallel to said first inverter (36) and said second inverter (39) and controlled by a latch pulse.

5. The liquid crystal display device as claimed in claim 4, wherein said level conversion means (15-1 to 15-n) and said latch means (16-1 to 16-n) further comprise a fifth switch (40) provided between input and output of said second inverter (39) and controlled by said level shift pulse additionally.

6. The liquid crystal display device as claimed in claim 4 or claim 5, wherein said reference voltage has an electric potential of approximately (VH - VL)/2, in which VH stands for the high level of input digital data and VL stands for the low level of the input digital data.

7. The liquid crystal display device as claimed in claim 1 or claim 2, wherein said level conversion means (15-1 to 15-n) is a level shift circuit for shifting the level of the digital signal sampled by said sampling means (12-1 to 12-n) to the power voltage level of said horizontal driving circuit system.

8. The liquid crystal display device as claimed in claim 7, wherein said pulse generation means (11) is a horizontal scanning circuit which generates also a level shift pulse to be supplied to said level shift circuit (15-1 to 15-n).

9. The liquid crystal display device as claimed in claim 1 or claim 2, wherein said sampling means (12-1 to 12-n) is a switch element provided correspondingly to a column line.

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F I G. 1

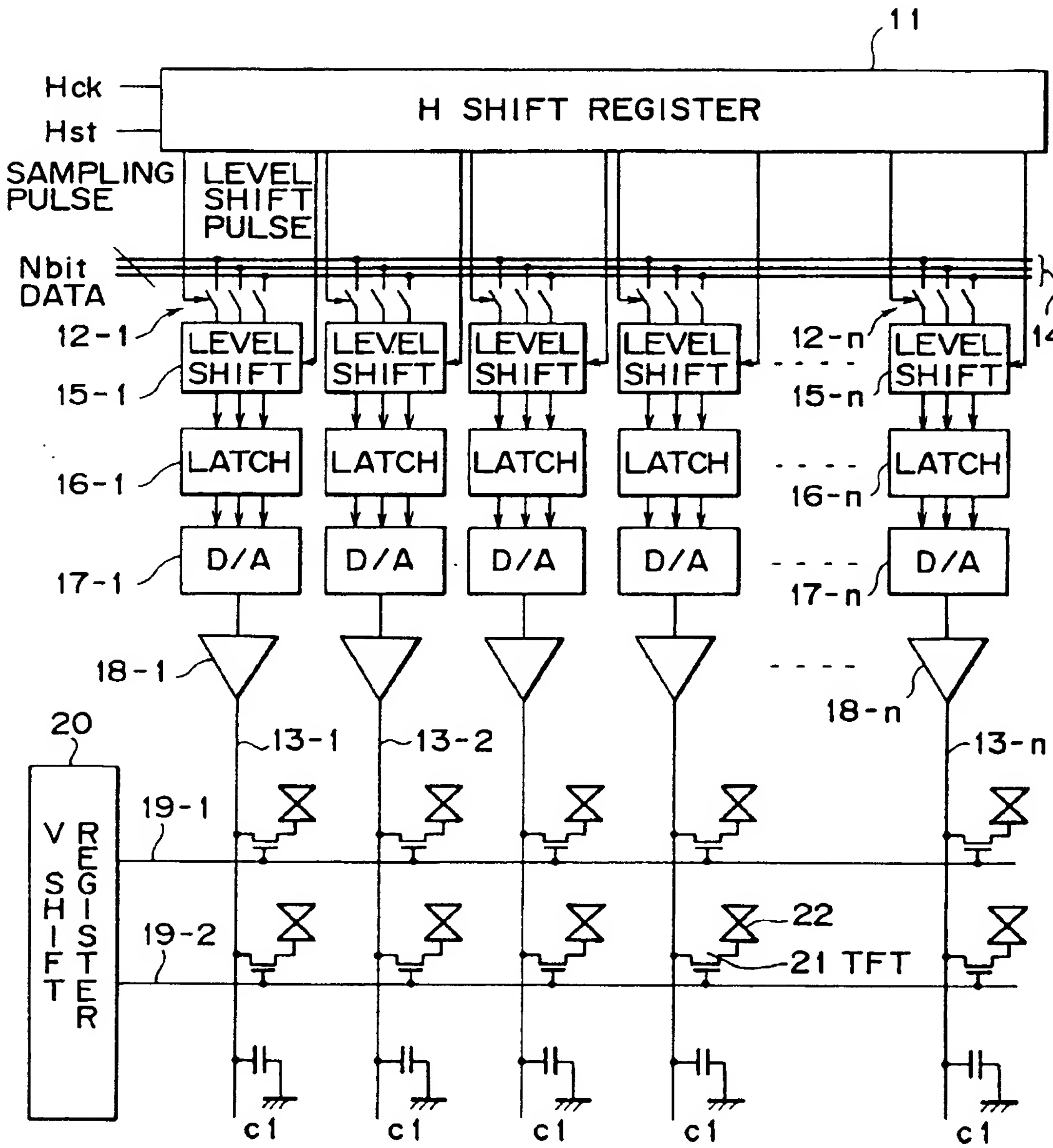

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FIG. 2

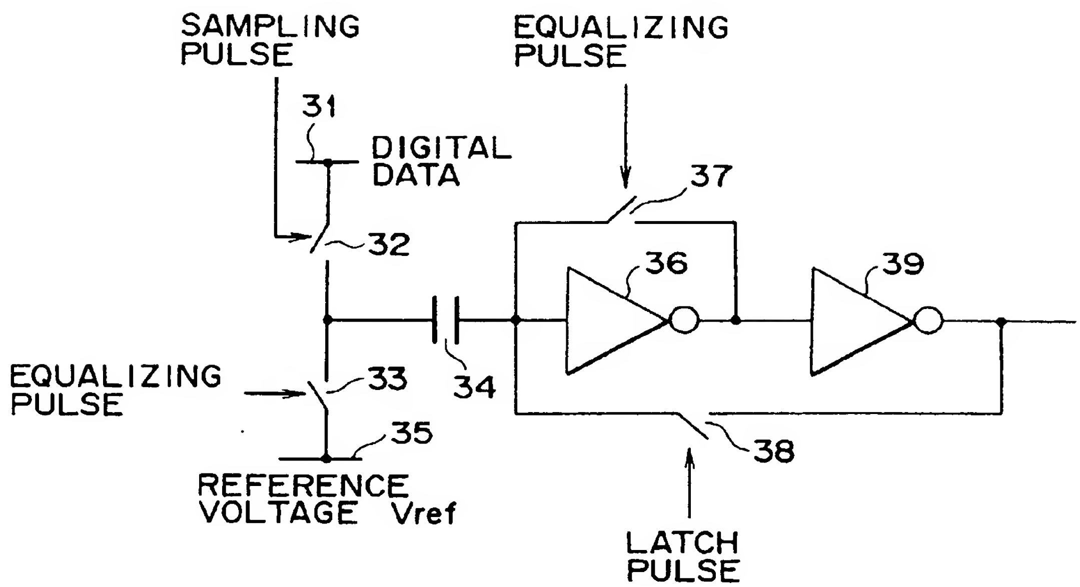
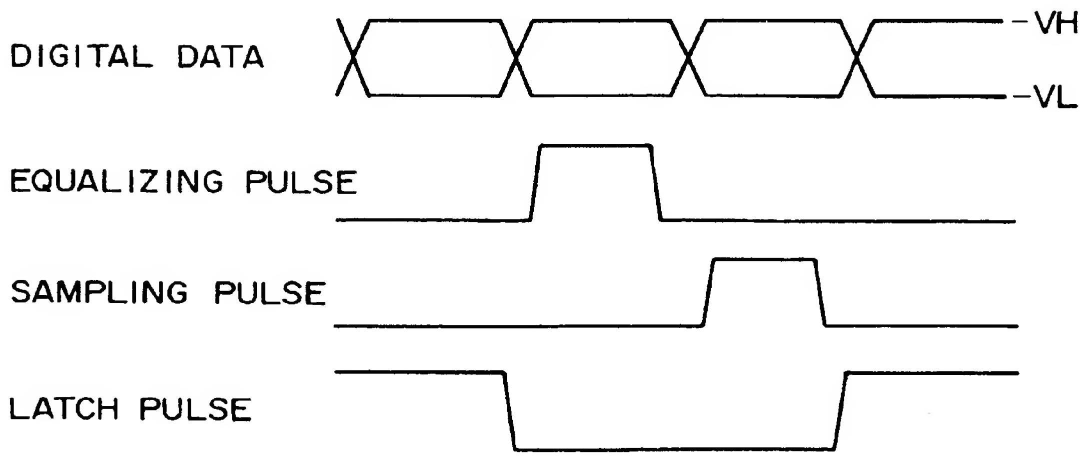


FIG. 3



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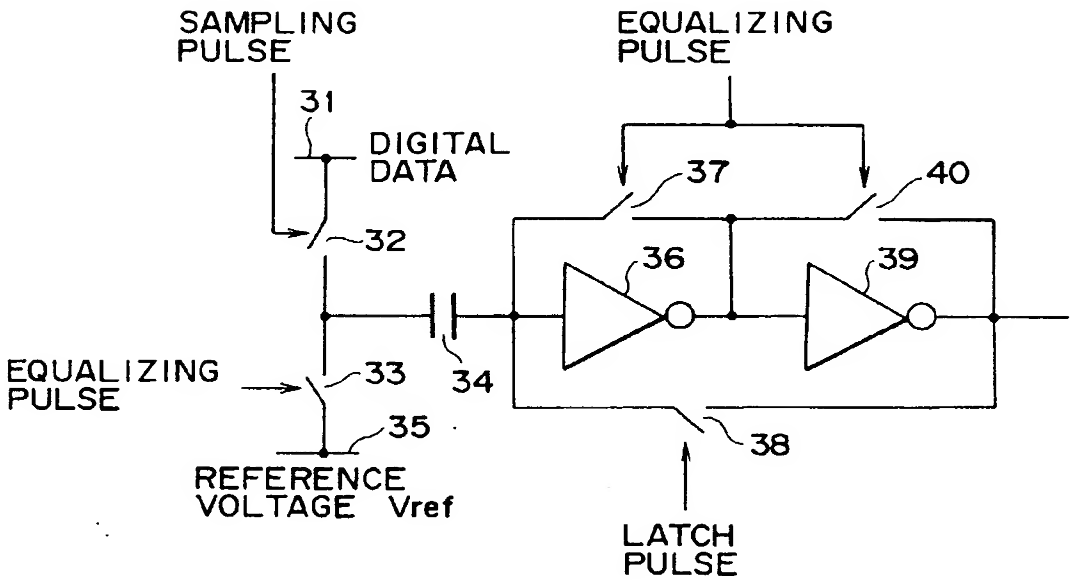
F I G. 4



F I G. 6

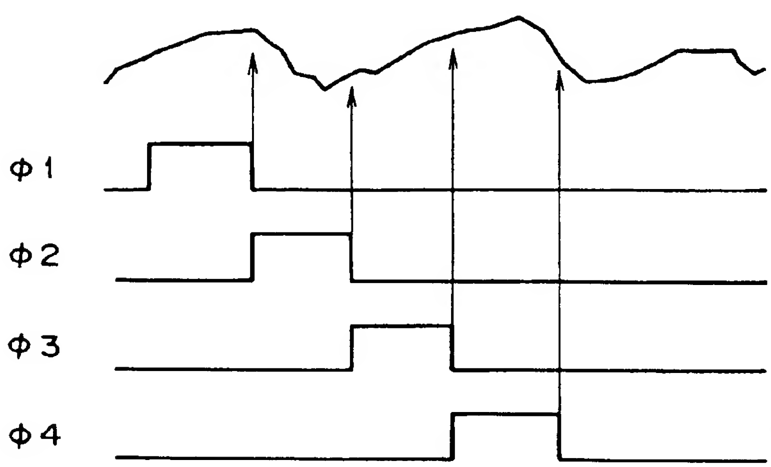


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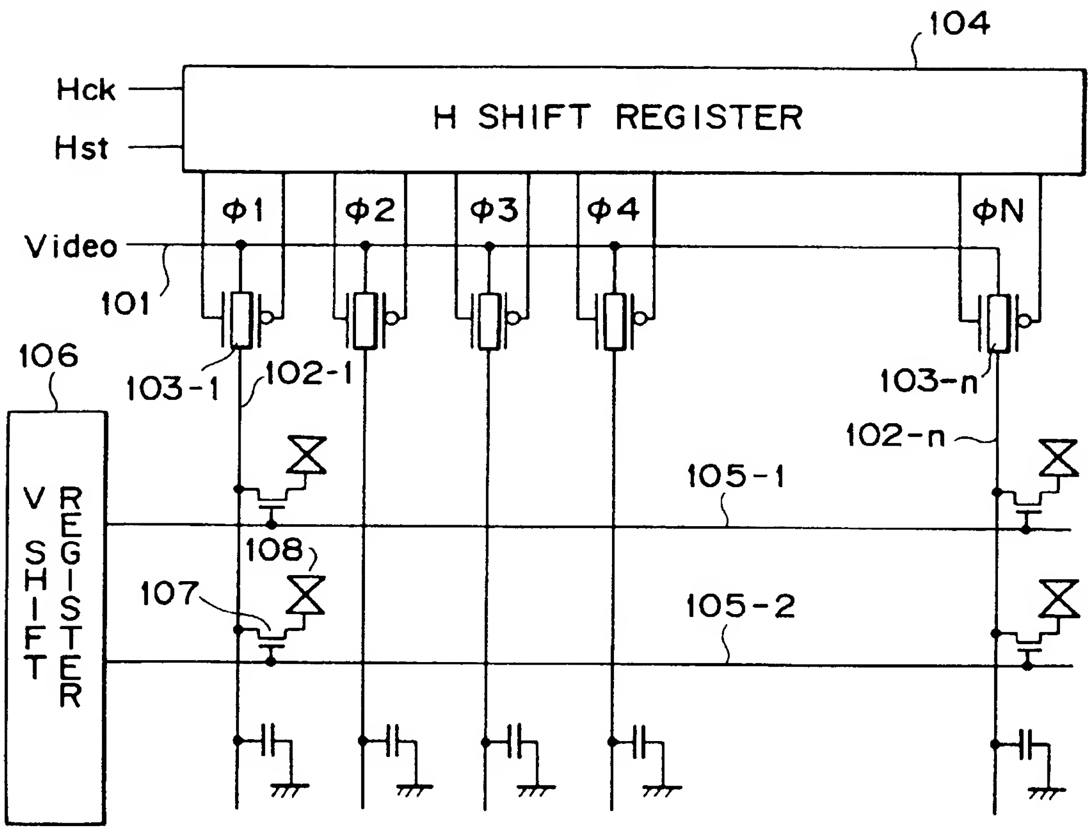
FIG. 5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Φ2
Φ3
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Video
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